What is claimed is:

1. A PLL circuit in which a phase comparator, a loop filter, a voltage control oscillator and a frequency divider are successively loop-connected, said PLL circuit comprising: operation stoppage detecting means for detecting that PLL operation has stopped; and control means for, when said operation stoppage detecting means detects stoppage of operation, controlling the voltage control oscillator such that an oscillation frequency of the voltage control oscillator is low.

2. A PLL circuit according to claim 1, wherein said operation stoppage detecting means is a means for detecting presence/absence of an output signal of the frequency divider.

3. A PLL circuit according to claim 1, wherein said operation stoppage detecting means is a means for detecting whether or not a control voltage of the voltage control oscillator is a value that oscillates a frequency which is greater than or equal to a predetermined value.

4. A PLL circuit according to claim 1, wherein said operation stoppage detecting means is a means for detecting whether or not an oscillation frequency of the voltage control oscillator is value higher than a predetermined value.

5. A PLL circuit according to any one of claims 1 through 4, wherein said control means is a means for switching an output of the phase comparator to a value at which an oscillation frequency of the voltage control oscillator decreases.

6. A PLL circuit according to any one of claims 1 through 4, wherein said control means is a means for switching a comparison signal inputted to the phase comparator such that an oscillation frequency of the voltage control oscillator decreases.